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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/623,101 | 07/18/2003 | Guillermo Rozas | TRAN-P072 | 2896 |

45590 7590 01/27/2009

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| EXAMINER | |
|---|---|
| PETRANEK, JACOB ANDREW | |
| ART UNIT | PAPER NUMBER |
| 2183 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 01/27/2009 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/623,101 | ROZAS ET AL. | |
| | Examiner | Art Unit | |
| | Jacob Petranek | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-14 are pending.

2. The office acknowledges the following papers:

Claims and arguments filed on 11/19/2008.

### *New Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 5-7, 9-12, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larsen (U.S. 5,115,500).

5. As per claim 1:

Larsen disclosed a method of processing an instruction, said method comprising:

fetching said instruction using a corresponding address from a memory unit (Larsen: Figure 2, column 5 lines 34-67 continued to column 6 lines 1-40)(An instruction is fetched from the I-Store 2 using an address from the memory unit (Instruction Address Register, IAR 3).), wherein a first meaning is associated with said instruction stored at said corresponding address by the same processor when a first plurality of bits from said corresponding address is concatenated with said instruction (Larsen: Figure 2, column 4 lines 56-67 continued to column 5 lines 1-12 and column 5 lines 34-67 continued to column 6 lines 1-40)(A first meaning is given to an instruction stored at a

corresponding address if the address ends in '111,' which indicates a type two instruction.), and wherein a second meaning is associated with said instruction stored at said corresponding address by said same processor when a second plurality of bits from said corresponding address is concatenated with said instruction (Larsen: Figure 2, column 4 lines 56-67 continued to column 5 lines 1-12 and column 5 lines 34-67 continued to column 6 lines 1-40)(A second meaning is given to an instruction stored at a corresponding address if the address ends in anything but '111,' which indicates a type one instruction. These two meanings are dependent upon what the corresponding address is when decoded by the decoder. It's obvious to one of ordinary skill in the art that the two different types of instructions are different since the objective of the invention of Larsen is to allow the execution of two or more different machine types on a single processor.);

concatenating a portion of said corresponding address to said instruction to form an extended instruction (Larsen: Figure 2, column 3 lines 52-64 and column 5 lines 34-67 continued to column 6 lines 1-40)(The three bits are selected to determine how the instruction will be decoded regardless of if the instruction came from the memory units that store type 1 instructions or the memory units that store type 2 instructions.), and wherein said concatenation increases a number of instructions in an instruction set (Larsen: Figure 2, column 4 lines 56-67 continued to column 5 lines 1-12)(The instruction set architecture is comprised of both the type 1 and type 2 instruction sets. Prior to the concatenation, only a single type of instructions was allowed to execute. However, now with the concatenation, the number of instructions can at the maximum

double the number of opcodes available for instructions. Type 1 and type 2 are different instructions, which results in increasing the number of instructions available to the overall instruction set architecture of the processor.); and

executing said extended instruction, wherein said portion of said corresponding address determines a meaning for said extended instruction from said possible meanings (Larsen: Figure 2, column 5 lines 34-67 continued to column 6 lines 1-40)(The instruction is decoded and then executed with one of the possible meanings, which is dependent on the extended instruction formed from the concatenation.).

6. As per claim 2:

Larsen disclosed the method as recited in claim 1 wherein said portion is an address bit (Larsen: Fig. 2, col. 5, line 34 to col. 6, line 40).

7. As per claim 3:

Larsen disclosed the method as recited in claim 1 wherein said portion is a plurality of address bits (Larsen: Fig. 2, col. 5, line 34 to col. 6, line 40).

8. As per claim 5:

Larsen disclosed a method of handling an instruction, said method comprising:

generating said instruction, wherein a first meaning is associated with said instruction stored at said corresponding address by a same processor when a first plurality of bits from said corresponding address is concatenated with said instruction (Larsen: Figure 2, column 4 lines 56-67 continued to column 5 lines 1-12 and column 5 lines 34-67 continued to column 6 lines 1-40)(A first meaning is given to an instruction stored at a corresponding address if the address ends in '111,' which indicates a type

two instruction.), and wherein a second meaning is associated with said instruction stored at said corresponding address by said same processor when a second plurality of bits from said corresponding address is concatenated with said instruction (Larsen: Figure 2, column 4 lines 56-67 continued to column 5 lines 1-12 and column 5 lines 34-67 continued to column 6 lines 1-40)(A second meaning is given to an instruction stored at a corresponding address if the address ends in anything but '111,' which indicates a type one instruction. These two meanings are dependent upon what the corresponding address is when decoded by the decoder. It's obvious to one of ordinary skill in the art that the two different types of instructions are different since the objective of the invention of Larsen is to allow the execution of two or more different machine types on a single processor.);

storing said instruction at a particular address in a memory unit such that a portion of said particular address enables determination of a meaning for said instruction from said possible meanings (Larsen: Figure 2, column 2 lines 21-54 and column 5 lines 34-67 continued to column 6 lines 1-40.); and

before executing said instruction, fetching said instruction using said particular address from am memory unit and concatenating said portion of said particular address to said instruction (Larsen: Fig. 2, col. 3, lines 52-64 and col. 5, line 34 to col. 6, line 40)( The three bits are selected to determine how the instruction will be decoded regardless of if the instruction came from the memory units that store type 1 instructions or the memory units that store type 2 instructions.), and wherein said concatenation increases a number of instructions in an instruction set (Larsen: Figure 2, column 4 lines 56-67

continued to column 5 lines 1-12)(The instruction set architecture is comprised of both the type 1 and type 2 instruction sets. Prior to the concatenation, only a single type of instructions was allowed to execute. However, now with the concatenation, the number of instructions can at the maximum double the number of opcodes available for instructions. Type 1 and type 2 are different instructions, which results in increasing the number of instructions available to the overall instruction set architecture of the processor.).

9. As per claim 6:

Claim 6 essentially recites the same limitations of claim 2. Therefore, claim 6 is rejected for the same reasons as claim 2.

10. As per claim 7:

Claim 7 essentially recites the same limitations of claim 3. Therefore, claim 7 is rejected for the same reasons as claim 3.

11. As per claim 9:

Larsen disclosed the method of as recited in claim 5 wherein said generating said instruction and said storing said instruction are performed by a compiler (Larsen: Column 1 lines 11-29)(Larsen disclosed that a compiler must be generated for each new machine. A compiler by definition translates high-level language into object code prior to the execution of a program. Thus, a compiler generates instructions that are executable on a processor. A compiler is also defined as any program that transforms one set of symbols into another by following a set of syntactic and semantic rules. As shown in figure 2, a rule for the processor is that type 2 instructions can only be placed

in memory locations ending with '111.' Thus, it's obvious to one of ordinary skill in the art that this is a semantic rule that the compiler of Larsen must follow and correctly place all type 2 instructions only in memory locations ending with '111' and place all type 1 instructions at other memory locations. Thus, the compiler also stores instructions in memory places.).

12. As per claim 10:

Claim 10 essentially recites the same limitations of claim 1. Therefore, claim 10 is rejected for the same reasons as claim 1.

13. As per claim 11:

Claim 11 essentially recites the same limitations of claim 2. Therefore, claim 11 is rejected for the same reasons as claim 2.

14. As per claim 12:

Claim 12 essentially recites the same limitations of claim 3. Therefore, claim 12 is rejected for the same reasons as claim 3.

15. As per claim 14:

Claim 14 essentially recites the same limitations of claim 9. Therefore, claim 14 is rejected for the same reasons as claim 9.

16. Claims 4, 8 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larsen (U.S. 5,115,500), in view of ("390 Principles of Operation"), herein referred to as IBM.

17. As per claim 4:

Larsen disclosed the method as recited in claim 1.

Larsen failed to teach wherein the plurality of possible meanings include an integer type of instruction and a floating point type of instruction.

However, IBM disclosed wherein the plurality of possible meanings include an integer type of instruction and a floating point type of instruction (IBM: Pages 7-1 to 7-6, 9-1 to 9-4, and 9-8 to 9-9)(The combination results in type 1 instructions being the instructions of the IBM 390 ISA. Thus, one of the plurality of possible meanings could be a integer instruction from the 390 ISA or a floating point instruction from the 390 ISA.).

Larsen disclosed two separate types of instruction used, but failed to disclose what types of ISA's are used. Since the Larsen patent was produced from IBM, one of ordinary skill in the art would have been motivated to look at IBM ISA's for more information on what types of instructions are supported. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the IBM 390 ISA onto the processor of Larsen.

18. As per claim 8:

Claim 8 essentially recites the same limitations of claim 4. Therefore, claim 8 is rejected for the same reasons as claim 4.

19. As per claim 13:

Claim 13 essentially recites the same limitations of claim 4. Therefore, claim 13 is rejected for the same reasons as claim 4.

***Response to Arguments***

20. The arguments presented by Applicant in the response, received on 11/19/2008 are not considered persuasive.

21. Applicant argues "As a result, an instruction stored in a location has only one type. Associating the instruction with a different type requires the instruction to be stored in a different location of a memory component. As such, Larsen fails to teach or suggest fetching an instruction using a corresponding address from a memory unit, wherein a first meaning is associated with the instruction stored at the corresponding address by a same processor when a first plurality of bits from the corresponding address is concatenated with the instruction, and wherein a second meaning is associated with the instruction stored at the corresponding address by the same processor when a second plurality of bits from the corresponding address is concatenated with the instruction, as claimed" for claim 1.

This argument is not found to be persuasive for the following reason. Larsen can still read on the claim 1 because of the way that the first and second meanings are claimed. The first meaning and second meaning are dependent upon a first and second plurality of bits. Looking at claim 1, both the first and second plurality of bits can be interpreted as being element 40, where for example a first meaning is if $b_2b_1$=00 and a second meaning is $b_2b_1$=01. Such a claim is no different from what is disclosed by Larsen, where a first and second meaning are dependent upon the fetched address that is to be decoded.

The examiner previously stated in an interview with the applicant on 11/20/2008 that if the first meaning was from element 30 and the second meaning was from element 40 in figure 1, then the claim would overcome the rejection of Larsen. The examiner notes that the following amendment to the independent claim 1 would over come the rejection:

fetching said instruction using a corresponding address from a memory unit, wherein a first meaning is associated with said instruction stored at said corresponding address by the same processor when a first [[plurality of bits]] bit from said corresponding address is concatenated with said instruction, and wherein a second meaning is associated with said instruction stored at said corresponding address by said same processor when a second plurality of bits from said corresponding address is concatenated with said instruction, wherein the fetched instruction can have the first meaning or second meaning dependent upon said concatenated first bit or second plurality of bits;

This amendment makes clear that a first meaning is supposed to come from element 30 in figure 1 and a second meaning is supposed to come from element 40 in figure 1. It also ensures that two different meanings are for the exact same fetched instruction address, where the different meanings are dependent upon which bit(s) are concatenated to the fetched instruction address.

## ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

Jacob Petranek
Examiner, Art Unit 2183